WHAT IS CLAIMED IS:

1. A threshold voltage stabilizer, for use with a MOS transistor having a body effect associated therewith, comprising:

a body well located in a substrate;

a source located in said body well; and

a stabilization region, positioned below said body well, said threshold voltage stabilizer being configured to provide a stabilization voltage to said stabilization region to increase a depletion region within said body well and thereby restrict said body effect to stabilize a threshold voltage of said MOS transistor.

2. The threshold voltage stabilizer as recited in Claim 1 wherein said depletion region limits an expansion of a channel depletion region within said body well.

3. The threshold voltage stabilizer as recited in Claim 1 wherein said body well is not directly connected to said source.

4. The threshold voltage stabilizer as recited in Claim 1 wherein said stabilization voltage is independent of a backgate bias voltage applied to said body well.

5. The threshold voltage stabilizer as recited in Claim 1 wherein said stabilization region further includes a side stabilization region that contacts said stabilization region.

6. The threshold voltage stabilizer as recited in Claim 5 wherein said side stabilization region is adjacent said body well and forms a stabilization ring about said body well.

7. The threshold voltage stabilizer as recited in Claim 1 wherein said body well is doped with a first dopant and said stabilization region is doped with a second dopant opposite to said first dopant.

8. The threshold voltage stabilizer as recited in Claim 7 wherein a concentration of said first dopant ranges from about $5E15/cm^3$ to $5E16/cm^3$ and a concentration of said second dopant ranges from about $5E18/cm^3$ to $2E19/cm^3$.

9. The threshold voltage stabilizer as recited in Claim 1 wherein said stabilization voltage is provided by a variable voltage source configured to deliver a voltage sufficient to stabilize said threshold voltage.

10. A method of manufacturing a threshold voltage stabilizer for use with a MOS transistor having a body effect associated therewith, comprising:

forming a body well in a substrate;

forming a source in said body well;

creating a stabilization region wherein at least a portion of said stabilization region is located below said body well; and

configuring said threshold voltage stabilizer to provide a stabilization voltage to said stabilization region to increase a depletion region within said body well and thereby restrict said body effect to stabilize a threshold voltage of said MOS transistor.

11. The method as recited in Claim 10 wherein said configuring said threshold voltage stabilizer allows said depletion region to limit an expansion of a channel depletion region within said body well.

12. The method as recited in Claim 10 wherein forming said body well allows electrical isolation from said source.

13. The method as recited in Claim 10 wherein said creating a stabilization region further includes creating a side stabilization region that contacts said stabilization region.

14. The method as recited in Claim 13 wherein said side stabilization region is adjacent said body well and forms a stabilization ring about said body well.

15. The method as recited in Claim 10 wherein said forming said body well includes doping said body well with a first dopant and said forming said stabilization region includes doping said stabilization region with a second dopant opposite to said first dopant.

16. The method as recited in Claim 15 wherein a concentration of said first dopant ranges from about $5E15/cm^3$ to $5E16/cm^3$ and a concentration of said second dopant ranges from about $5E18/cm^3$ to $2E19/cm^3$.

17. The method as recited in Claim 10 further including providing said stabilization voltage from a variable voltage source that delivers a voltage sufficient to stabilize said threshold voltage.

18. An integrated circuit, comprising:

memory cells located on a semiconductor substrate;

MOS transistors located on said semiconductor substrate, said transistors having a body effect associated therewith;

threshold voltage stabilizers, for use with said transistors, located on said semiconductor substrate wherein each includes:

a body well located in said semiconductor substrate;

a source located in said body well; and

a stabilization region, positioned below said body well, said threshold voltage stabilizer providing a stabilization voltage to said stabilization region to increase a depletion region within said body well and thereby restrict said body effect to stabilize a threshold voltage of said MOS transistor; and

interconnects interconnecting said memory cells, said MOS transistors and said threshold voltage stabilizers to form an operative integrated circuit.

19. The integrated circuit as recited in Claim 18 wherein said depletion region limits an expansion of a channel depletion region within said body well.

20. The integrated circuit as recited in Claim 18 wherein said body well is not directly connected to said source.

21. The integrated circuit as recited in Claim 18 wherein said stabilization voltage is substantially independent of a backgate bias voltage applied to said body well.

22. The integrated circuit as recited in Claim 18 wherein said stabilization region further includes a side stabilization region that contacts said stabilization region.

23. The integrated circuit as recited in Claim 22 wherein said side stabilization region is adjacent said body well and forms a stabilization ring about said body well.

24. The integrated circuit as recited in Claim 18 wherein said stabilization voltage is provided by a variable voltage source that delivers a voltage sufficient to stabilize said threshold voltage.

25. The integrated circuit as recited in Claim 18 wherein said threshold voltage stabilizers form a portion of said memory cells.